

Yoav Lavi - CV

Summary

- Numerous VLSI designs and architectures, including some 20 patents and pending applications.
- Recent Specialty areas include serial video interface and ISP

In the last decade:

- Built and managed Tower Semiconductor VLSI Design Center
- Designed EPROM and Flash chips
- Started and ran Cellular3G R&D center
- Designed a UMTS baseband chip
- Represented Transchip (today Samsung) in MIPI Camera and D-PHY working groups
- Defined and optimized VLSI architectures for several companies
- Prepared dozen of patent disclosures and patent applications Played a major role in new digital camera VLSI architectures
- Participated and contributed to MIPI industry consortium for mobile processor interface
- Developed the SVR – high quality MIPI CSI2/SMIA CCP2 compliant Receiver and Transmitter IP core (the CSI2 receiver IP is the only one available with MIPI IOL certificate)

Patents Summary (Partial)

- U.S. 4,377,855, 1983: "Content Addressable Memory". Sole inventor
- U.S. 4,697,241, 1987: "Hardware Logic Simulator". Sole inventor
- U.S. 6,108,240, 2000: "Implementation of EEPROM using intermediate gate voltage to avoid disturb conditions". Co-inventor
- U.S. 6,256,231, 2001: "EEPROM array using 2-bit non-volatile memory cells and method of implementing same". Co-inventor
- U.S. 6,453,407, 2002: "Configurable Long Instruction Word architecture and Instruction Set". Main inventor
- U.S. 6,339,540, 2002: "Content-addressable memory for virtual ground flash architectures". Sole inventor
- U.S. 6,396,896, 2002: "Implementation of functions of multiple successive bits of a shift register". Sole inventor
- U.S. Published Application 20020138532: "Simplified circuit for correlating binary and non-binary sequences ", Sole inventor
- U.S. Published Application 20010021126: "EEPROM array using 2-bit non-volatile memory cells and method of implementing same". Co-inventor
- J.P. 6,250,620, 1992 "Programmable Format Video Memory". Co-inventor.
- PCT WO 99/42922: "An Apparatus for and Method of Executing Instructions of a Program" (this is the Configurable Long Instruction Word for the CARMEL DSP). Main inventor
- PCT/IL/2005/081629: Novel Pre-decoding Scheme for semiconductor memory. (Published patent application)
- PCT/IL2005/046237 – Efficient Binary CAM Architectures – filed PCT application

Summary of Professional History

- **1972 -1977: Ministry of Defense, State of Israel.** Advanced System design projects
- **1977-1978 – Intel.** VLSI designer for some of the top-selling microprocessor peripheral chips

- **1978-1984 – National Semiconductor.** Co-founder NS Israel Design Center. Defined and designed (with others) one of the most advanced microprocessor family of the time – the NS32000, including some 10 VLSI chips – microprocessors and peripherals.
- **1984-1990 – Simulog.** Inventor of a new architecture for Hardware Logic Simulator based on a multitude of full custom VLSI chips. Founded and managed a company to exploit the technology, including VLSI, System and Software development. The top line product, built jointly with Amdahl Corporation, U.S.A, was acknowledged to be the fastest simulator in existence.
- **1990 – Self Employed.** Designed and built a telephone encryption unit, using Diffie-Hellmann algorithm with 521 bit numbers for key establishment, followed by randomtime-slice scrambling.
- **1990-1996 – i Sight.** Founded and managed the VLSI design group. Defined and designed multi-media chip and an Image Signal Processor (ISP) chip. At the time this was the only commercially available ISP outside Japan, outperforming all the Japanese competition.
- **1996-1997 – Consultant.** Played a key role in the architecture of the CARMEL - a high performance low power DSP core, aimed at high-end cellular applications, for Infineon and ICCOM. In addition, conducted a Feasibility Study for a single chip videoconferencing VLSI, on contract from NEC Electronics, and the RF interface unit for a mobile phone VLSI, on contract from an Israeli Spread-Spectrum company.
- **1997-1999 – Tower Semiconductor.** Founded and managed Tower Semiconductor VLSI Design Center. Designed and taped-out an EPROM product (jointly with WSI) and a FLASH product (jointly with Saifun), which sold for many millions of units. Invented a unique way to use the Flash technology for implementing ultra dense ternary content addressable memories (U.S. 6,339,540: "Content-addressable memory for virtual ground flash architectures"). Co-invented two patents in the area of Flash design.
- **1999-2003 – Cellular3G.** Co-founded and headed the R&D of Cellular3G. Developed a baseband processor for W-CDMA (UMTS), featuring very low power computation and compact design. Defined the architecture of the chip, and then led the design of the FPGA prototype, the ASIC, the L1 software, the GUI and the regression test system.
- **2004-Present – VLSI Plus.** Opened VLSI Plus — a boutique VLSI engineering house, specializing in VLSI Architectures, VLSI patents and VLSI cores.

Patents area: activities include editing of some 50 patents for several customers, (including, in three cases, adding features and thus becoming a co-inventor). Submission of three patent applications in the Memory field, based on own new inventions.

VLSI Architecture area: Filled the position of Chief Architect for Transchip, in charge of defining the architecture of the company's image-sensor and ISP chips. Played an active role in MIPI, defining the interface of future cell-phone cameras to mobile processors. Optimized VLSI architectures of several companies, saving a considerable amount of the area and power consumption. Developed a special processors, compression algorithms, encryption techniques and more, for a variety of customers.

VLSI Cores area: Developed MIPI interface IP cores – the SVT Serial Video Transmitter, the SVR Serial Video Receiver, and more.