CSI2 Serial Video Transmitter (SVT-CSCP)

Information Brief

Introduction

This document is a short description of VLSI Plus (www.vlsiplus.com) CSI2 / CCP dual-mode Serial Video Transmitter (SVT-CSCP) for video streams.

The SVT-CSCP is designed to interface smoothly with commonly used CMOS Image Sensors. Optional add-ons can be used to expand the basic image-sensor functionality and allow other features like low-power communication, and others. A single clock lane and one or two data lanes are supported.

Overview

MIPI (Mobile Industry Processor Interface) is an industry consortium, which defines standards for the interface between modules of a mobile device. Two of those standards are DPHY, defining the physical level of high speed communication, and CSI2, defining the Camera Serial Interface.

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When in CSI mode, the SVT-CSCP supports CSI2.

Functionality highlights include:

- One clock lane, and One (standard) or two (optional) data lanes ;
- Up to 1Gbps per lane;
- Supports RAW8, RAW10, RAW12 and User-Defined 8-bit formats, with other CSI2 standards available as an option
- CRC and ECC generation
- Programmable timing parameters
- Bare-Core of less than 3,000 interfaces directly with RAW-Bayer image sensors
- Extensions to support:
    - Escape-Mode signaling
    - Registered parameters
    - Additional FIFO

SMIA (Standard Mobile Imaging Architecture) is an industry consortium, which defines standards for mobile imager modules. SMIA standards encompass numerous aspects of the imager, allowing pin level compatibility. One of those standards is CCP2 - high speed communication between the sensor and a host application processor.

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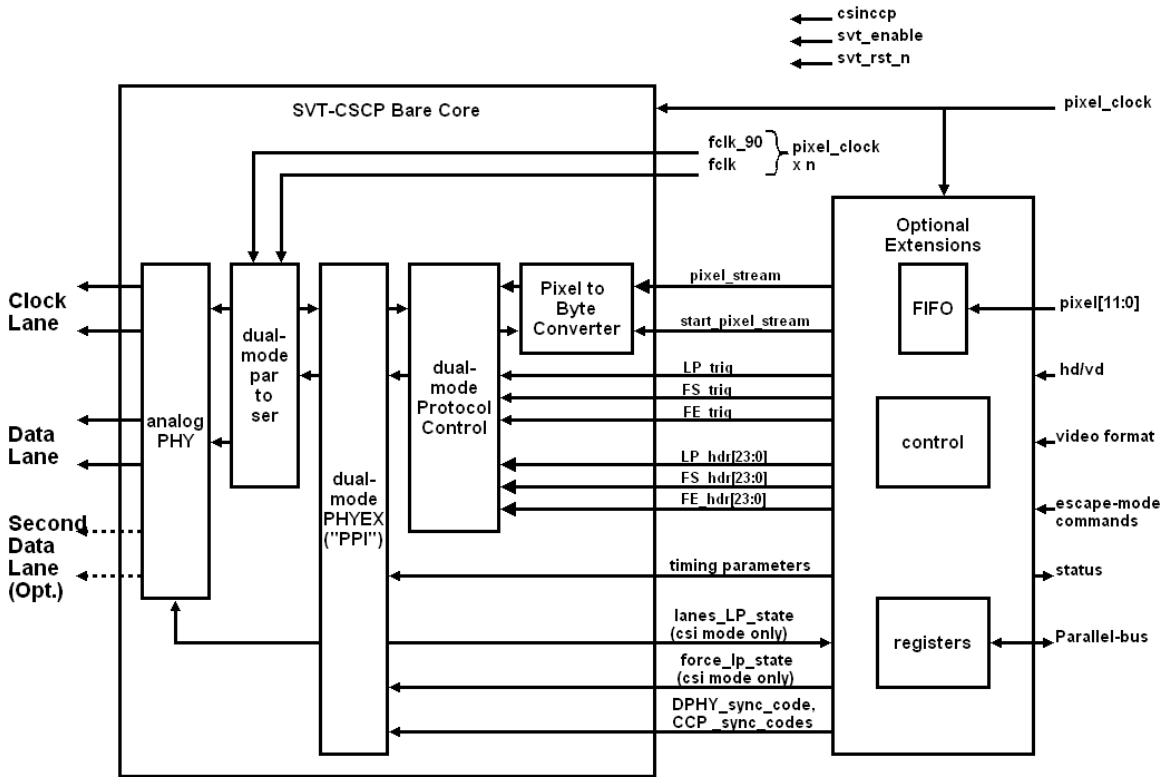
When in CCP mode, the SVT-CSCP supports CCP2.

SMIA – mode Functionality highlights include:

- Class 0, 1 and 2;
- Up to 650Mbps;
- Supports all applicable SMIA data formats (RAW8, RAW10, User-Defined 8-bit)
- Supports RAW12 format (beyond the SMIA scope)

An input pin ***csinccp*** selects the mode of operation

Simplified Block Diagram



The figure above depicts a simplified block diagram of the SVT-CSCP.

The block marked ***SVT-CSCP Bare Core*** generates CRC and ECC codes, converts the pixels to byte, interfaces between clock domains and controls the analog PHY according to the MIPI D-PHY and to CCP specification.

The Bare-Core, of approximately 3,000 gates, is all that is needed for basic image sensor CSI / CCP functionality. The image sensor should send parallel video stream, in RAW8, RAW10 RAW12 or user-defined 8-bit (e.g. JPEG). The pixel stream should be preceded by an LP-trigger pulse, typically generated HBLANK time prior to the pixel stream. In addition, the image sensor should generate Frame-Start and Frame-End trigger pulses.

The image sensor provides pixel-clock input, toggling at the pixel scan frequency. In addition, the image sensor also provides FCLK and FCLK_90 signals (FCLK only is needed for CCP mode). FCLK is a high speed DDR clock toggling at the required bit rate (that is, 500MHz for 1GBPS). FCLK_90 lags FCLK by 90 degrees. FCLK and FCLK_90 are typically generated by a PLL, which multiplies pixel-clock by n – the number of bits per pixel divided by 2.

Both FCLK and FCLK_90 are input to a compact parallel-to-serial circuit, which can achieve 1Gbps at most image sensor processes, without the need for process-dependant hard core technology.

The block marked “optional extensions” should be specified by the customer. In case the sensor cannot provide a LP-trigger prior to the beginning of the video stream, a FIFO can be added, which will take care to assert LP-trigger concurrently with the arrival of the first pixel, and hold enough pixels to allow for the MIPI-required delay.

In case it is desirable to hold all parameters in registers, a set of 32 bit registers is added, interfacing to the image sensor using standard parallel-bus synchronous protocol.

Other extensions can be added, to allow escape-mode LP signaling, video interleaving and more.