SVR-CSCP-F

Serial Video Receiver For FPGA Implementation

Information Brief

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Introduction

This document is a short description of VLSI Plus Serial Video Receiver (SVR-CSCP-F) – a dual SMIA CCP2 / MIPI^{R} CSI2 serial receiver for video streams, for FPGA implementations.

The SVR-CSCP-F is designed to interface smoothly with a parallel-input video board. It supports a clock lane and one or two data lanes while in CSI-2 mode. In CCP2 mode it fully supports a clock lane and a single data lane.

Overview

MIPI^{R} (Mobile Industry Processor Interface) is an industry consortium, which defines standards for the interface between modules of a mobile device. Two of those standards are DPHY, defining the physical level of high speed communication, and CSI2, defining the Camera Serial Interface.

SMIA (Standard Mobile Imaging Architecture) is an industry consortium, which defines standards for mobile imager modules. SMIA standards encompass several aspects of the imager, allowing pin level compatibility. One of those standards is CCP2 - high speed communication between the sensor and a host application processor.

The SVR supports both CCP2 and CSI2.

CSI2 Mode functionality highlights include:

- Configurable 1 or 2 data lanes;
- Up to 900 Mbps per lane;
- Interface signals as defined in Appendix B of MIPI^{R} CSI2 specifications;
- Support of all primary data formats, and more (see below).
- Optional support of CSI2 compressed-video formats
- Optional communication error counters, for BER evaluation

CCP2 Mode functionality highlight include:

- Class 0, 1 and 2;
- Up to 650Mbps
- Supporting all data formats as defined in Chapter 5 of the CCP2 Specifications, and more (see below);
- Receiver Behavior as recommended in Chapter 8 of the CCP2 Specifications.

System clocks

There are three clocks associated with the SVR-CSCP-F operation:

- HS-Clock – the clock derived from the serial video stream, and a divide-by-4 version whereof – HS_BYTE_CLK
- FCLK – internal SVR clock, at 240MHz
- DCLK – used to strobe the output pixels.

Flow of operation for CSI2

Short packets are decoded, and generate internal control information. Long packets (which represent pixel lines or data lines) are decoded from the input stream, and passed through the optional output buffer to the output pixel ports. Whenever the packet header is successfully received, the bytes which follow the header

are decoded to pixels, and input to the output buffer (if that option is specified), which regulates the rate and outputs uninterrupted stream of pixels.

The virtual channel of the packets is output on Channel_ID output.

Flow of operation for CCP2

The SVR converts incoming stream to pixels, and while doing so it constantly searches for an embedded sync pattern (0xFF0000X). When the pattern is found, one of SOF, EOF, SOL or EOL sync events is detected and signaled. The pixel stream, along with sync event indicators, is sent to the optional output buffer.

Pixels data type is programmed to the SVR in advance.

Some of the pixel lines contain data instead of pixels. Data will be output from the SVR in the same alignment as the pixels

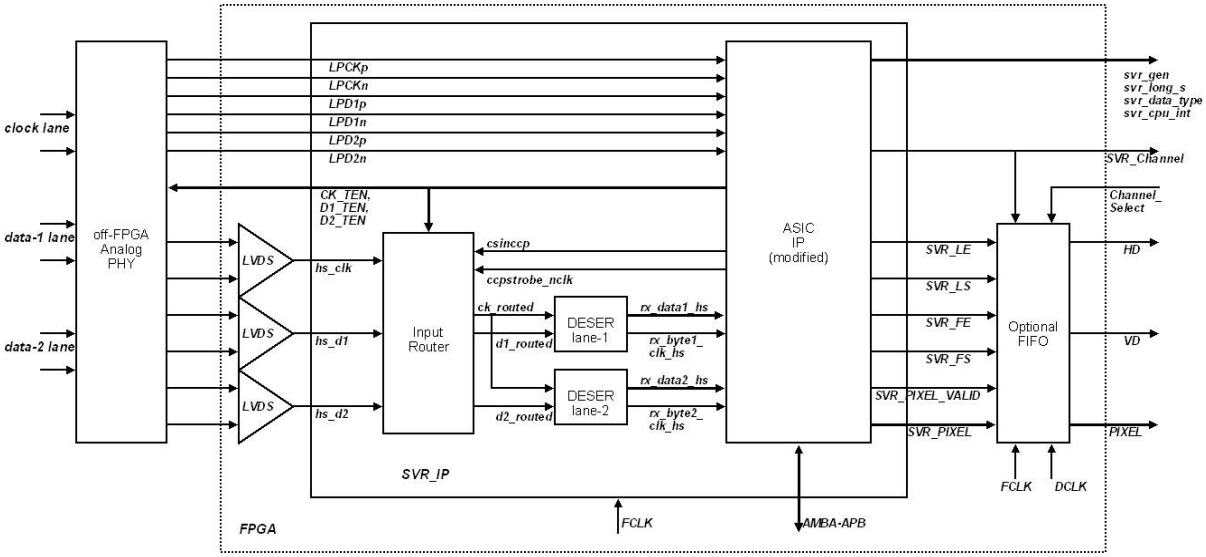
The virtual channel of the packets is output on Channel_ID bus.

Differences between SVR and SVR-F

The main differences between VLSI Plus SVR, ASIC version and the FPGA versions are summarized below:

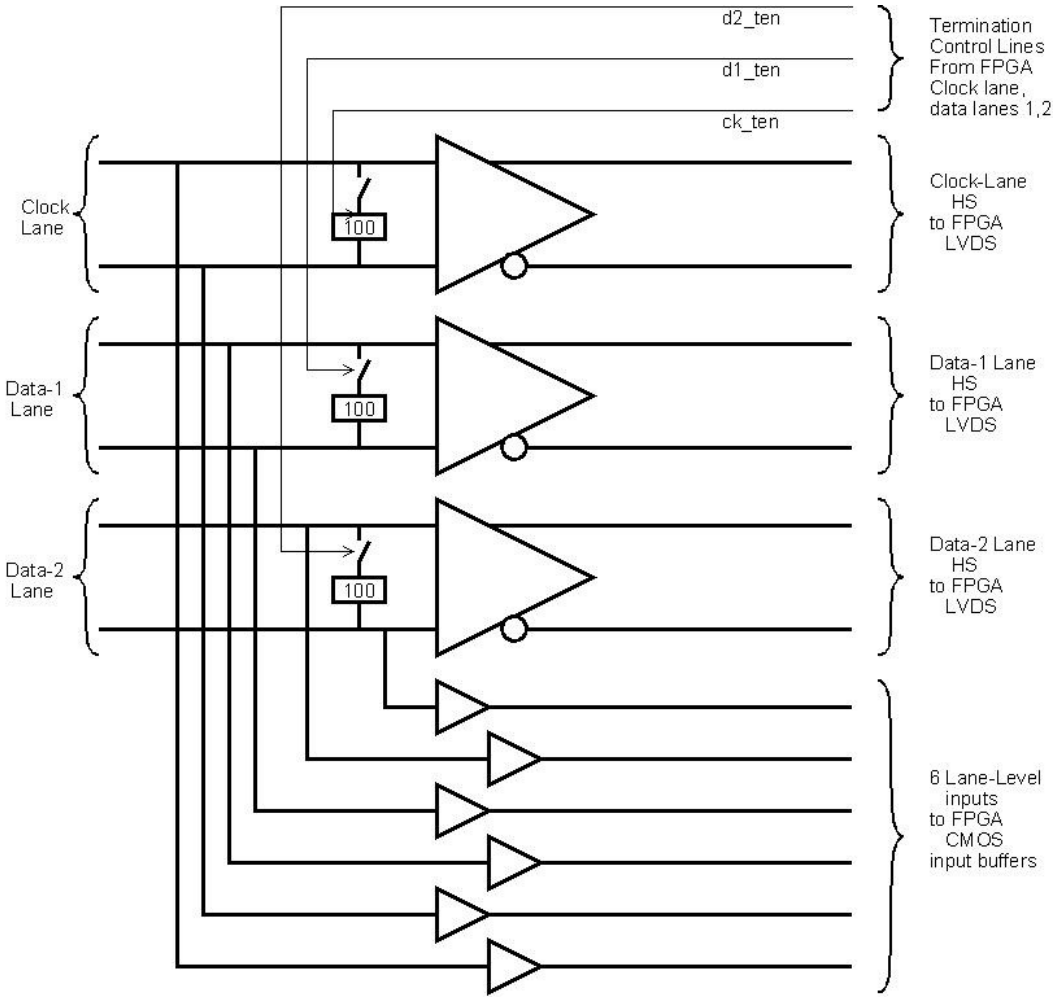
- Input to the FPGA is high speed differential lanes. Hence, the de-serialization is done in the FPGA, by fast digital circuits, as opposed to the ASIC version, where the serial to parallel conversion is done by the analog PHY
- When the Output-FIFO option is specified, a continuous output pixels stream is generated rather than pixels with Pixel_Valid qualifier
- Addition of Programmable synchronization codes, when such option is specified
- Automatic recovery from PHY error – while in the ASIC version, a governing CPU needs to clear the error flags and restart the SVR, the FPGA version flags an error, but recovers automatically from the error condition

SVR-CSCP-F Block Diagram



Off-FPGA Analog PHY

Off chip analog PHY circuits amplify the differential swing signaling, add LP level sensing and programmable termination, as depicted in the figure below. The three differential lanes are amplified by fast differential amplifiers, which receive the CCP and CSI input voltage levels and, in both cases, outputs standard differential LVDS level. Termination resistors on each of the three lanes are connected by FPGA control. In addition, the CMOS logic level of each of the six wires is sensed, and relayed to the FPGA.



VLSI Plus provides a full reference design for the analog PHY

SVR Registers

ADDRESS	NAME	FUNCTION
0x00	SVR_En_Reg	Enable SVR operation
0x04	SVR_Cfg_Reg	General Configuration
0x08	SVR_Timers_Cfg_Reg	Configuration of Timers
0x24	Int_Status_Register	Interrupt Status
0x28	Int_ Mask_Register	Interrupt Mask
0x30	Int_Read_and_Clear	Read and Clear Interrupt Status; Clear interrupt sources
0x40-0x5c	BER measurement registers	Optional set of counters, for BER measurement
0x80	EPHY_Level_Indication	Debug
0x84	Current_Packet_State	Debug
0x88	Last_Packet_Indication	Debug
0x90	Protocol_Level_Indication	Debug
0xA4	CSI_Sync Code	Optional
0xA8	CCP Sync Code	Optional
0xF8	IP Vendor Code	manufacturer ID assigned to VLSI Plus by MIPI^{R}
0xFC	Version	Unique 32 bit code for the current FPGA version