SVR-CS

CSI2
Serial Video Receiver

Information Brief

Introduction

This document is a short description of VLSI Plus (www.vlsiplus.com) SVR-CS – a MIPI CSI2 Serial Video Receiver for video streams.

The SVR-CS is designed to interface smoothly with commonly used Application Processors. It supports a clock lane and 2 data lanes.

Overview

MIPI (Mobile Industry Processor Interface) is an industry consortium, which defines standards for the interface between modules of a mobile device. Two of those standards are DPHY, defining the physical level of high speed communication, and CSI2, defining the Camera Serial Interface.

The SVR-CS supports MIPI CSI2 specifications.

Functionality highlights include:

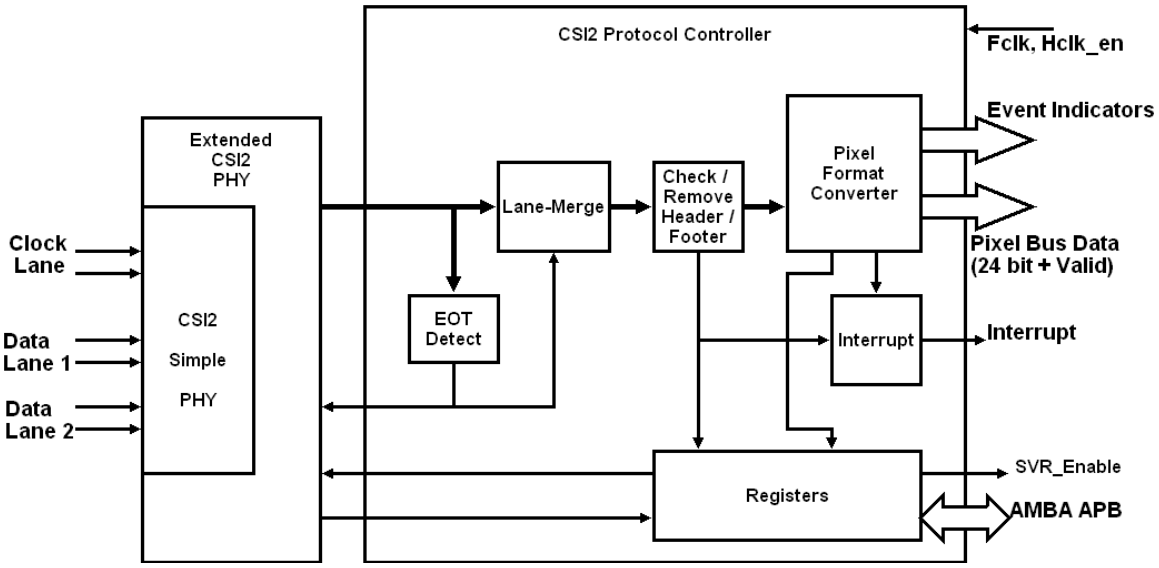
- Configurable 1 or 2 data lanes;
- Up to 1Gbps per lane;
- Interface signals as defined in Appendix B of MIPI CSI2 specifications;
- All CSI functionality implemented in hardware, freeing the CPU to other tasks
- Support of all data formats.
- Extensive set of registers, accessible by AMBA APB bus
- Programmable timing parameters

System clocks

The SVR-CS clock must be higher by at least 10% than the maximum data rate divided by 8. For two data lanes at 1Gbps each, this translates to 275MHZ.

The SVR-CS register file communicates with the Application Processor via a APB bus. APB clock is typically between 100 and 150MHZ.

Simplified Block Diagram



As illustrated above, The Extended PHY connects to a CSI1 PPI. Aligned pixel data from the Extended PHY is fed to Lane-Merge Logic, which merges the two lanes to serial packets of information. Further, special logic checks and removes headers and footers, including WC, ECC and CRC. The output of that unit now goes to a Format Converter, which modifies the format of the pixels to a simple parallel structure. The rearranged pixels are output on up to 24 pads (for RGB888 format), along with a Valid bit, to the Application Processor. Additional outputs are event indicators, one for every possible short or long packet reception event.

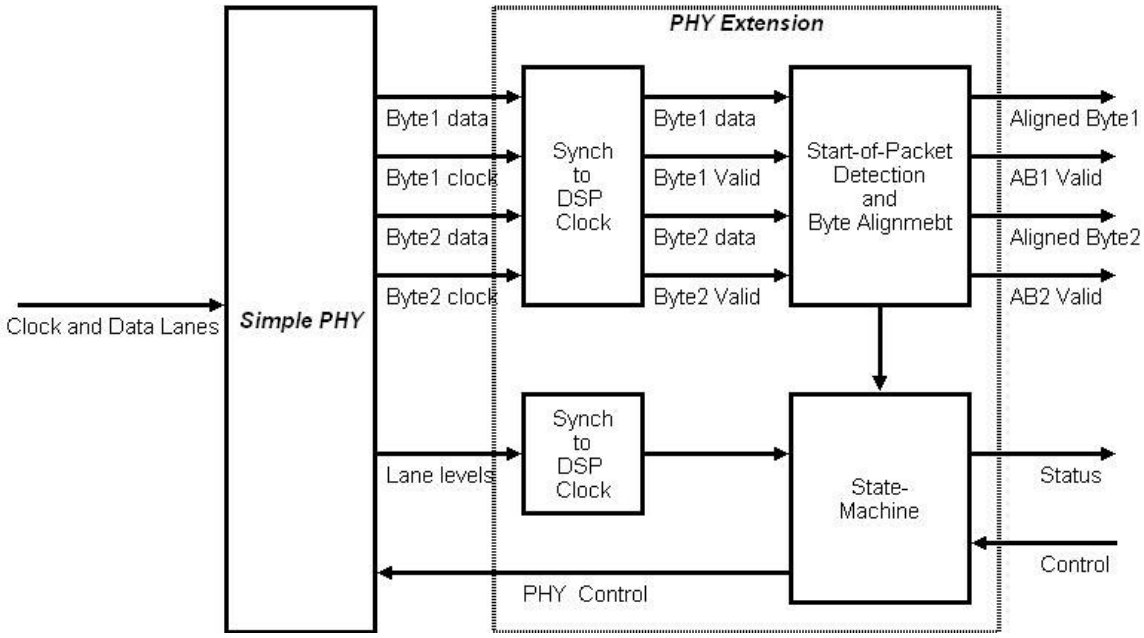
Besides the pixel-output bus, the SVR-CS communicates with the Application Processor via a 32 bit AMBA APB bus, which writes and reads SVR-CS registers. The registers contain configuration information, activation control codes, interrupt and other status information. Status is generated by the Extended PHY state machine, and by the header/footer check/remove unit.

Whenever an error event occurs an Interrupt output goes active The Application Processor will respond to the Interrupt, and read the corresponding Status register, to determine the reason for the interrupt.

Extended PHY Concept

As the PHY design is done separately for each target process, it is desirable to minimize its extent, and limit it to classical PHY tasks like differential receiver and de-serialization. In the MIPI D-PHY, additional functions are added, complicating the PHY design.

To solve this, VLSI Plus wraps a simple PHY, including legacy functions only, with synthesizable logic. The combined PHY and logic implement all D-PHY functions, as illustrated in the figure below:



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