



SVR-CSCP-4

Dual Mode 4-Lane CSI/CCP Serial Video Receiver

Information Brief

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Introduction

This document is a short description of VLSI Plus (www.vlsiplus.com) SVR-CSCP4 – a 4-lane Dual-Mode MIPI CSI2 / SMIA CCP2 Serial Video Receiver for video streams.

The SVR-CSCP4 is designed to interface smoothly with commonly used Application Processors. It supports a clock lane and a data lane when in CCP2 mode. In CSI2 mode it supports a clock lane and up to four data lanes.

Overview

SMIA (Standard Mobile Imaging Architecture) is an industry consortium, which defines standards for mobile imager modules. SMIA standards encompass numerous aspects of the imager, allowing pin level compatibility. One of those standards is CCP2 - high speed communication between the sensor and a host application processor.

MIPI (Mobile Industry Processor Interface) is an industry consortium, which defines standards for the interface between modules of a mobile device. Two of those standards are DPHY, defining the physical level of high speed communication, and CSI2, defining the Camera Serial Interface.

The SVR-CSCP4 supports both CCP2 and CSI2.

CSI2 Mode functionality highlights include:

- Configurable 1,2,3 or 4 data lanes;
- Up to 1Gbps per lane;
- Interface signals as defined in Appendix B of MIPI CSI2 specifications;
- All CSI functionality implemented in hardware, freeing the CPU to other tasks
- Support of all data formats.
- Extensive set of registers, accessible by AMBA APB bus
- Programmable timing parameters
- Optional support of CSI2 compressed-video formats
- Optional communication error counters, for BER evaluation

CCP2 Mode functionality highlight include:

- Class 0, 1 and 2;
- Up to 650Mbps;
- Supporting all data formats as defined in Chapter 5 of the CCP2 Specifications

- Receiver Behavior as recommended in Chapter 8 of the CCP2 Specifications.

A configuration bit (CSI/~CCP) defines the mode of operation.

System clocks

The SVR-CS4 clock must be higher by at least 5% than both the maximum pixel rate and the maximum bit rate divided by 16:

$$\text{Min}(F_{clk}) \geq 1.05 * (\max(L * \text{bps} / 16, \text{PPS}))$$

Where L is the number of lanes, bps is the bit rate per data lane, and PPS is the pixel-per-second rate.

Here are some examples:

RAW12, 2 lanes, 1Gbps

Pixel rate is $2 * 10^9 / 12 = 166.6\text{M}$.

Bit-rate/16 = $1\text{Gbps} * 2 / 16 = 125\text{M}$.

fclk > $166.6\text{M} * 1.05 = 175\text{MHz}$

YUV422 (16 bit per pixel), 4 lanes, 1Gbps

Pixel rate is $4 * 10^9 / 16 = 250\text{M}$.

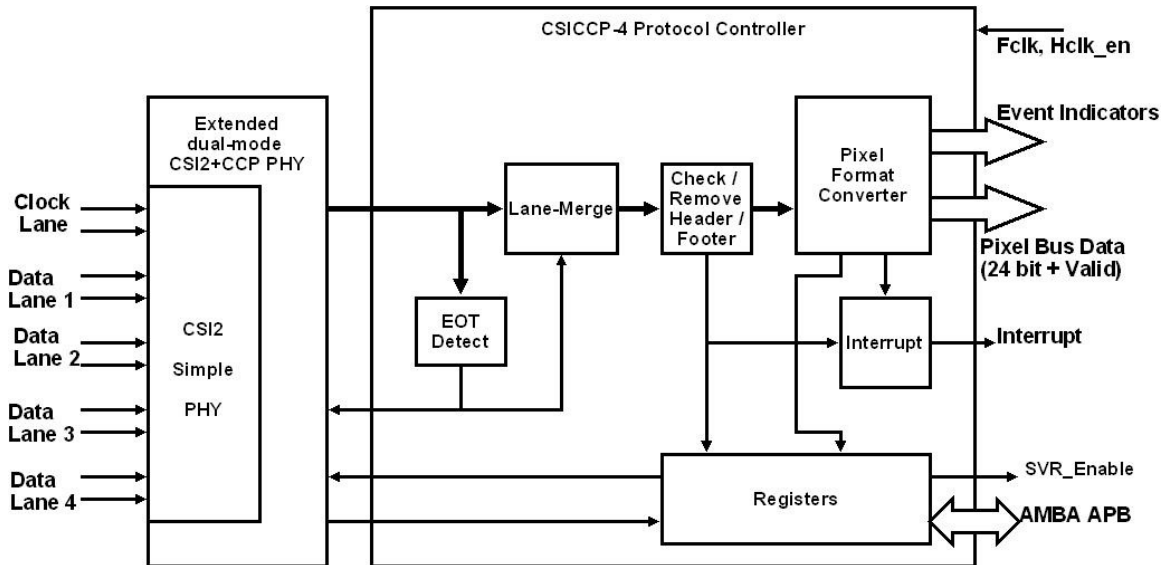
Bit-rate/16 = $1\text{Gbps} * 4 / 16 = 250\text{M}$

fclk > $250\text{M} * 1.05 = 262.5\text{MHz}$

The SVR-CSCP4 register file communicates with the Application Processor via an APB bus. APB clock is typically between 100 and 150MHz.

Simplified Block Diagram

The SVR-CSCP4 is based on the SVR-CSCP design, with the PHY, PHY-Extensions and Lane-Merger redesigned for 4-lane support, and redefinition of registers and busses.



As illustrated above, the 4-lane Extended PHY connects to a Dual Mode Protocol-Controller. Aligned pixel data from the Extended PHY is presented to the Lane-Merge Logic, which is active in multi-lane CSI2 modes only, and merges the active lanes to 16-bit-wide serial packets of information. Further, special logic checks and removes headers and footers, including WC, ECC and CRC. The output of that unit now goes to a Format Converter, which modifies the format of the pixels to a simple parallel structure. The rearranged pixels are output on up to 24 pads (for RGB888 format), along with a Valid bit, to the Application Processor. Additional outputs are event indicators, one for every possible short or long packet reception event.

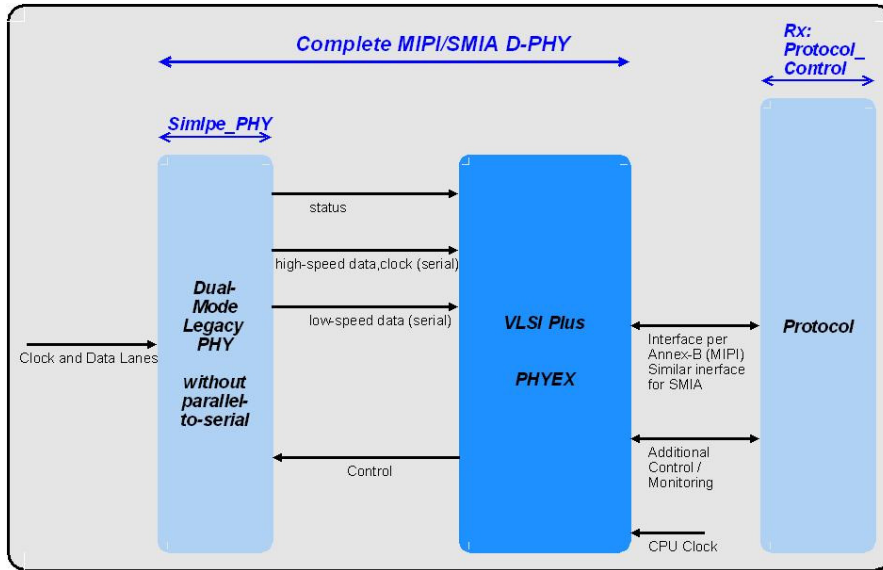
Besides the pixel-output bus, the SVR-CSCP4 communicates with the Application Processor via a 32 bit AMBA APB bus, which writes and reads SVR registers. The registers contain configuration information, activation control codes, interrupt and other status information. Status is generated by the Extended PHY state machine, and by the header/footer check/remove unit.

Whenever an error event occurs an Interrupt output goes active. The Application Processor will respond to the Interrupt, and read the corresponding Status register, to determine the reason for the interrupt.

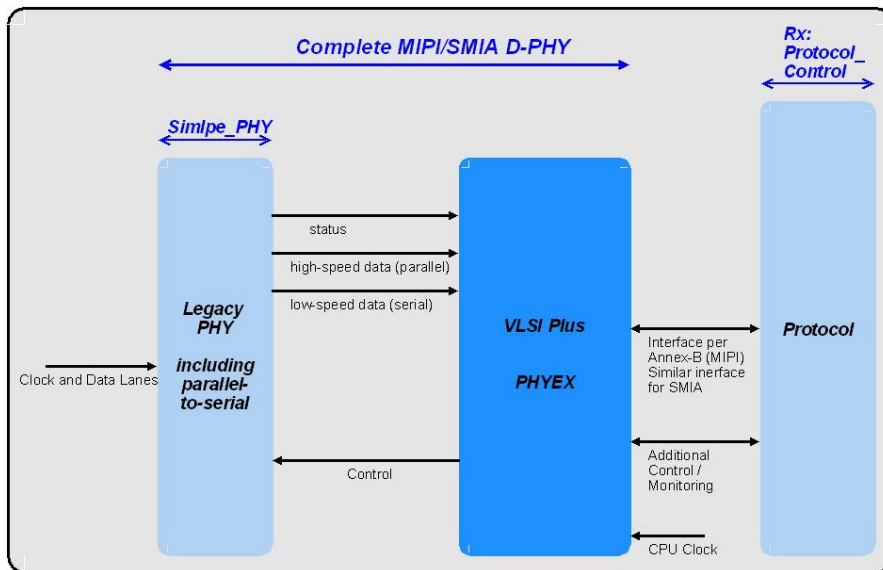
Extended PHY Concept

As the PHY design is done separately for each target process, it is desirable to minimize its extent, and limit it to classical PHY tasks like differential receiver and de-serialization. In the MIPI D-PHY, additional functions are added, complicating the PHY design.

To solve this, VLSI Plus wraps a simple PHY, including legacy functions only, with synthesizable logic. The combined PHY and logic implement all D-PHY functions, as illustrated in the figure below:



With advanced process technologies, of 90nm or less, the serial-to-parallel conversion can be optionally move to the synthesizable logic, deeming an even simpler analog PHY:



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